

1 / 30

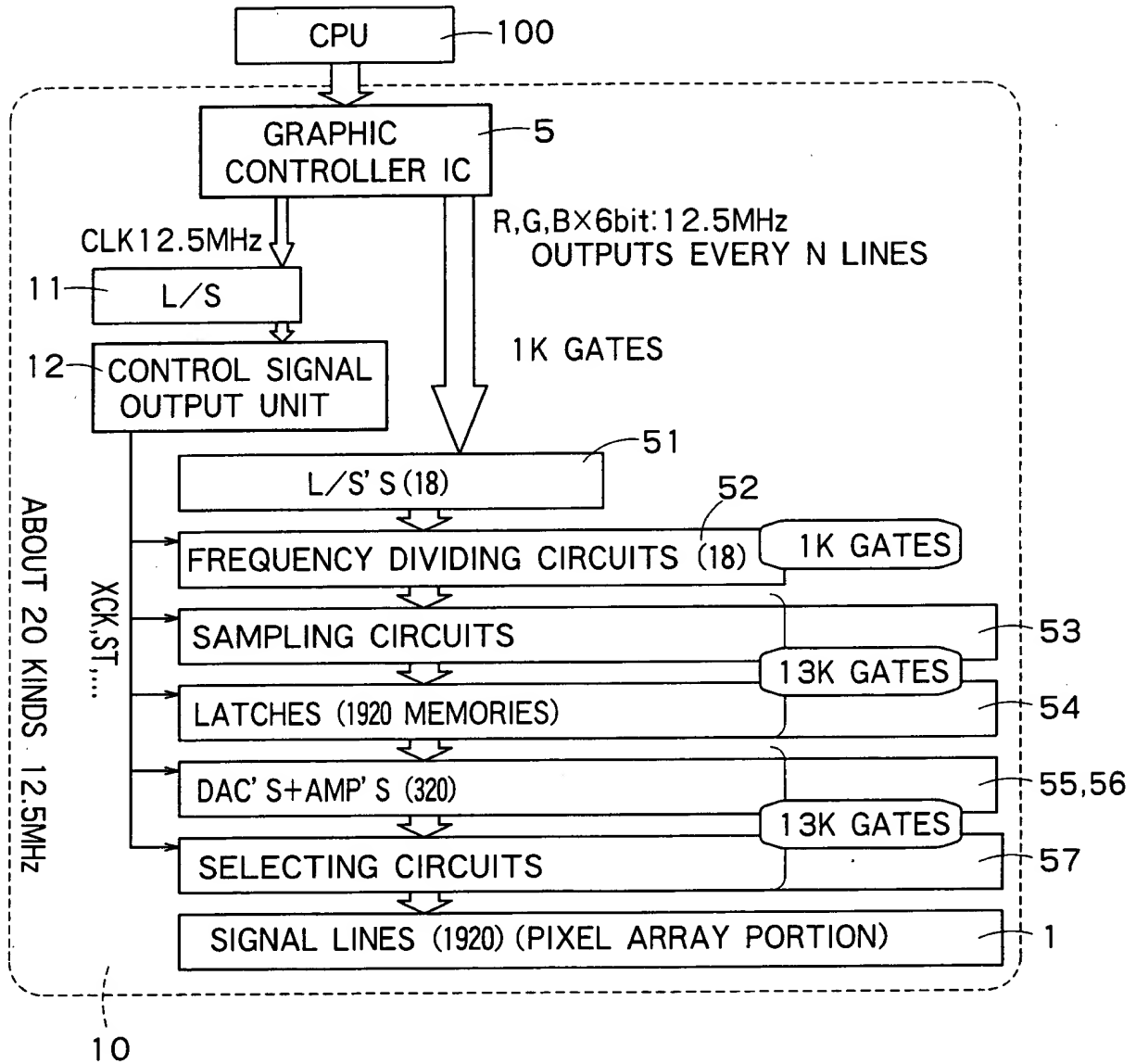
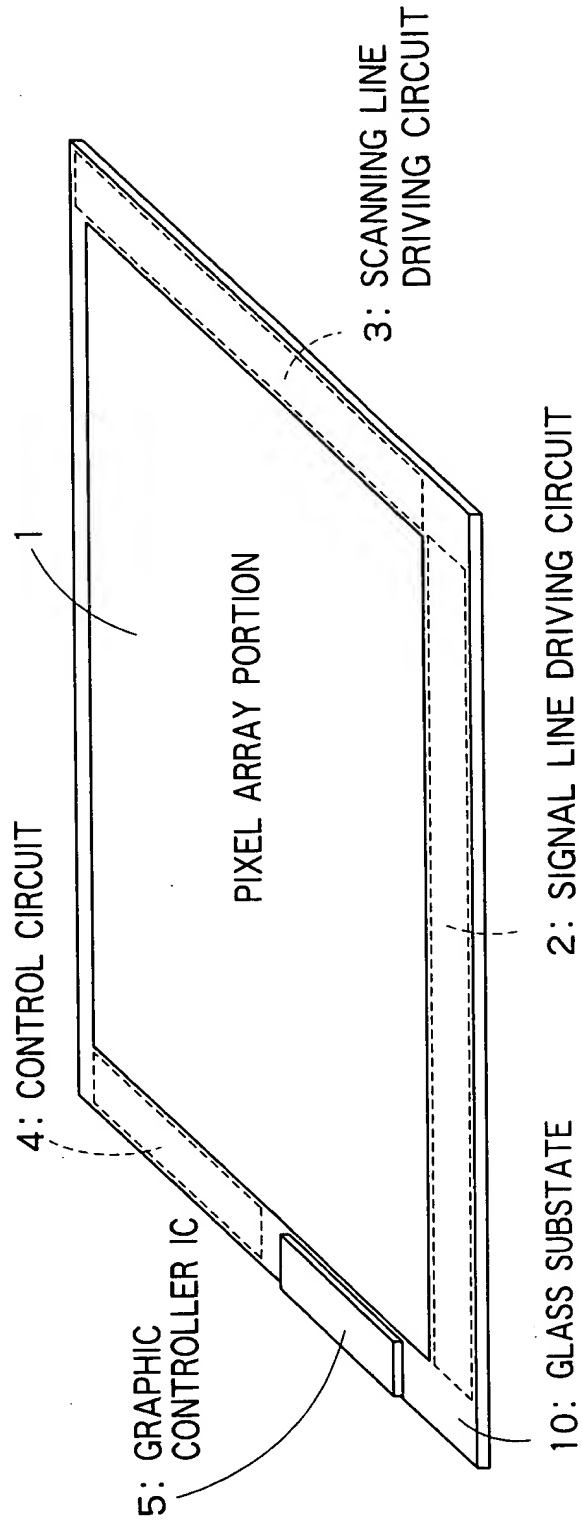


FIG. 1



F1G. 2

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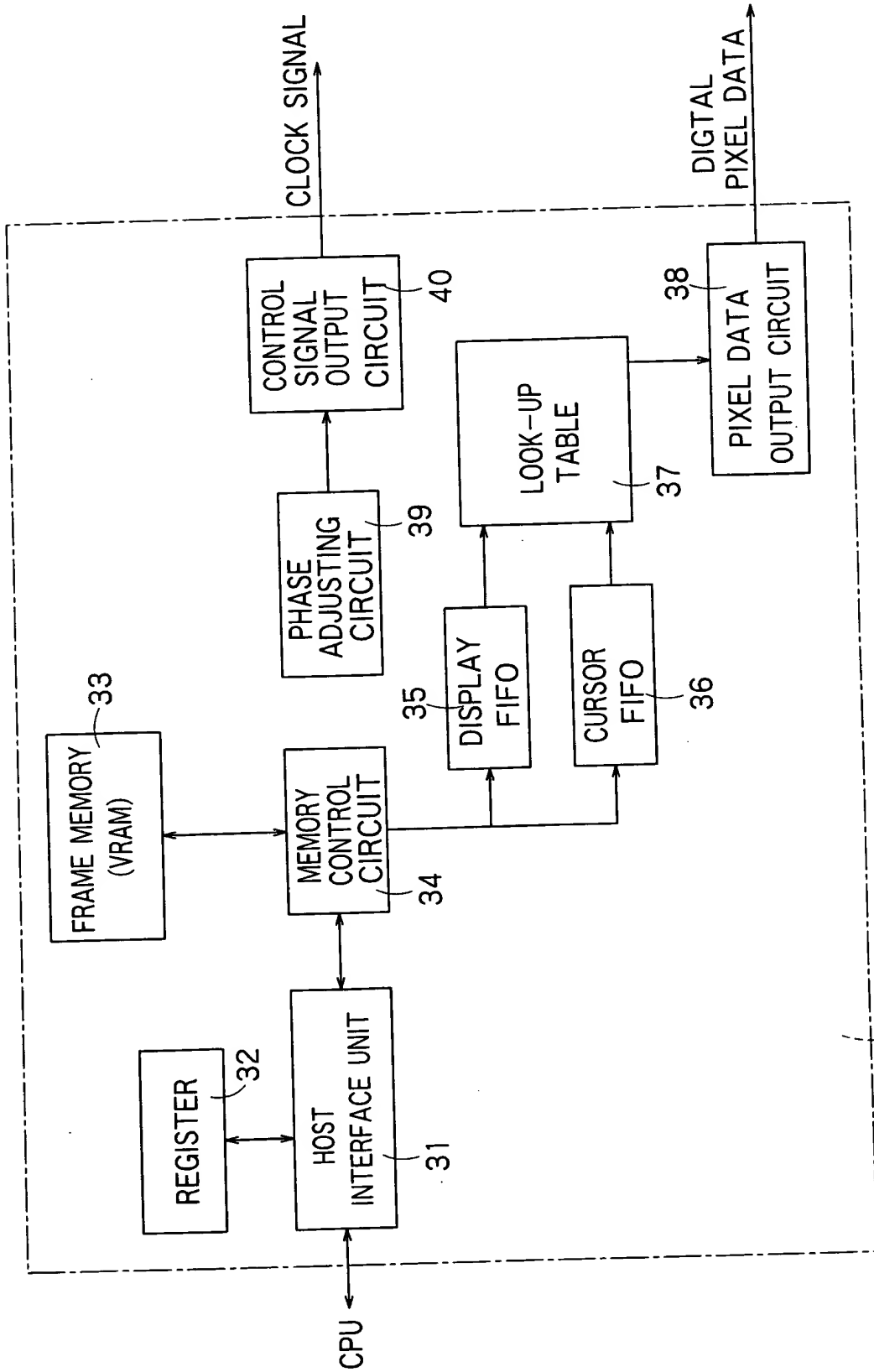


FIG. 3

5: GRAPHIC CONTROLLER IC

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FOZ2H0 00B24B60

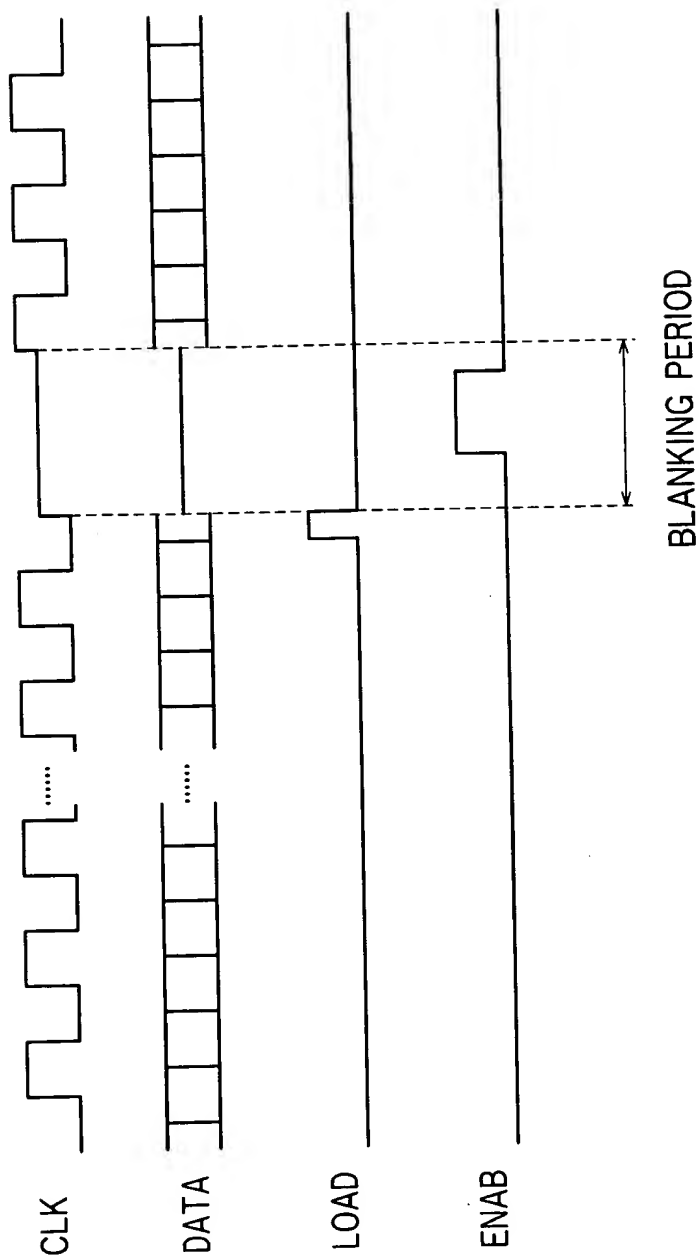


FIG. 4

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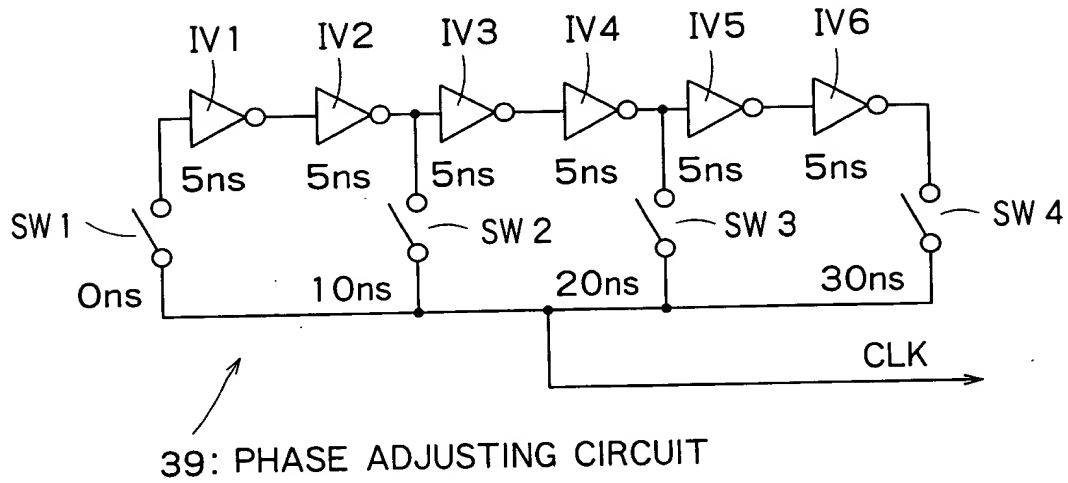


FIG. 5

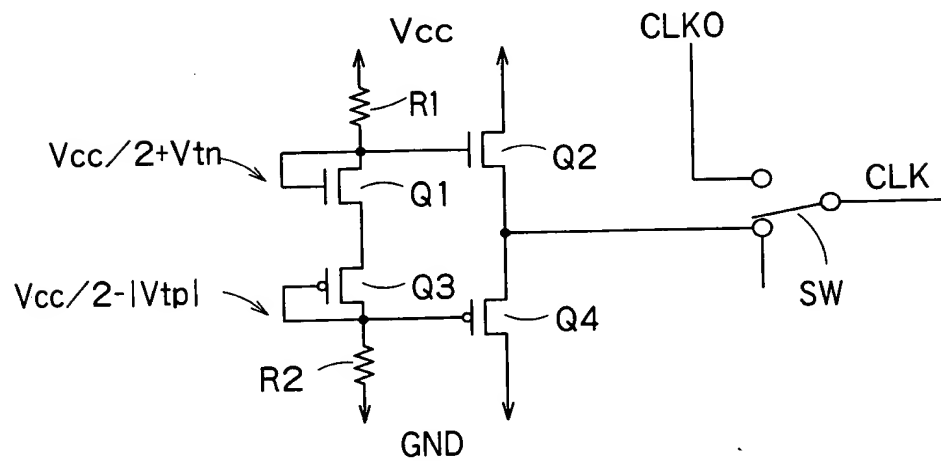


FIG. 6

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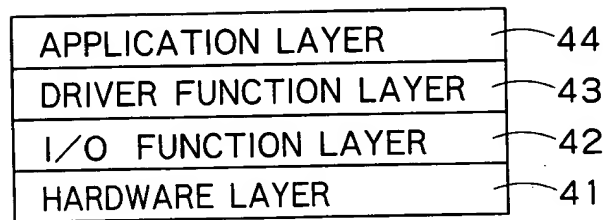


FIG. 7

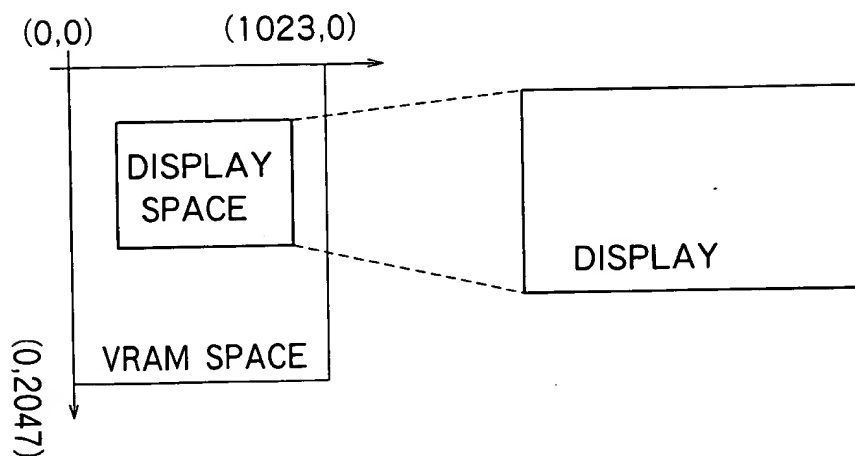


FIG. 8

09842800-042701

2: SIGNAL LINE DRIVING CIRCUIT

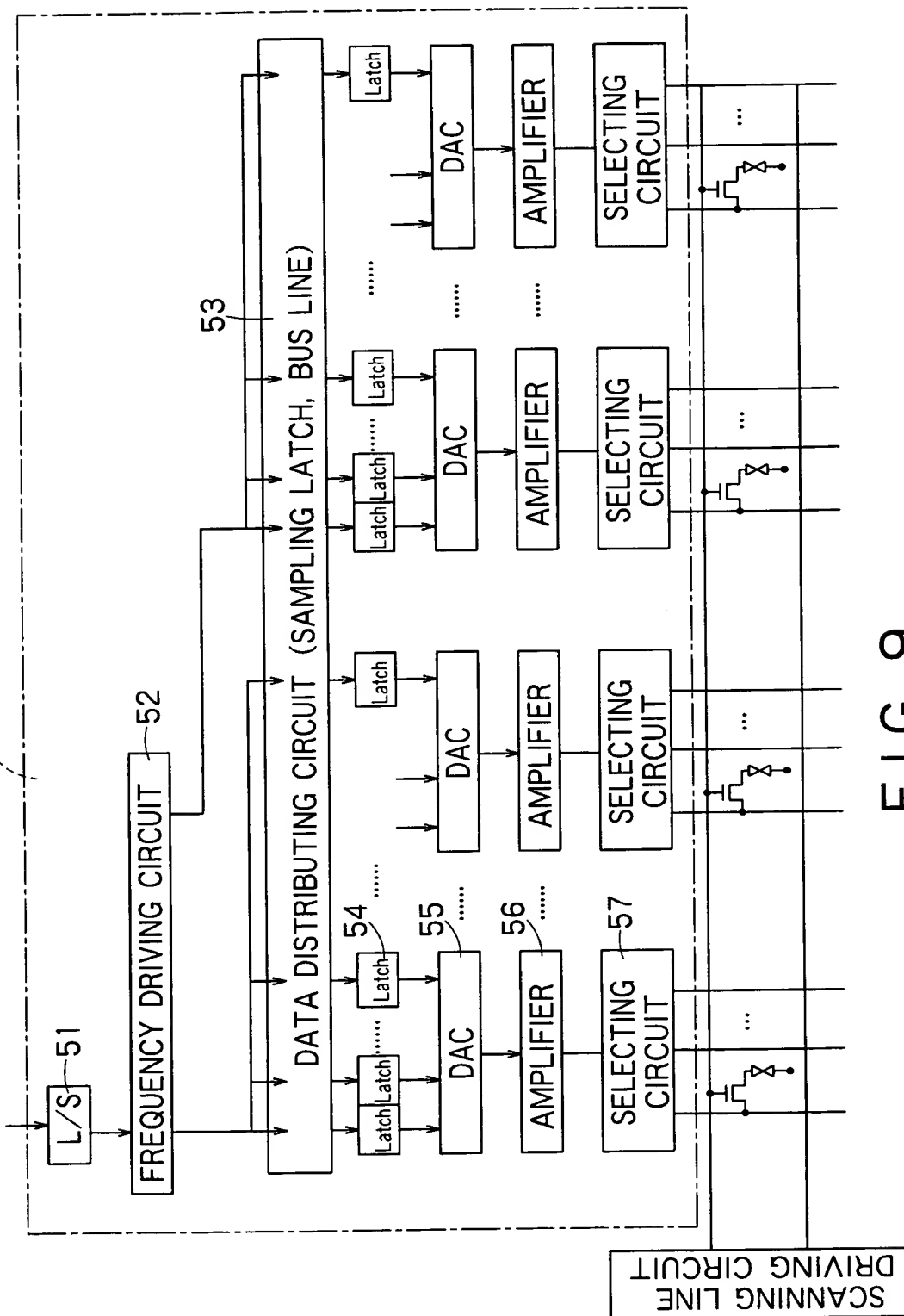


FIG. 9

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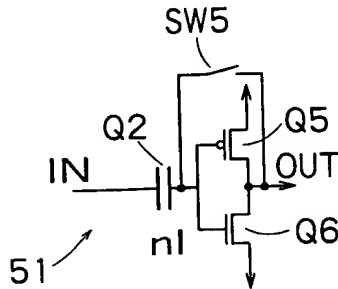


FIG. 10

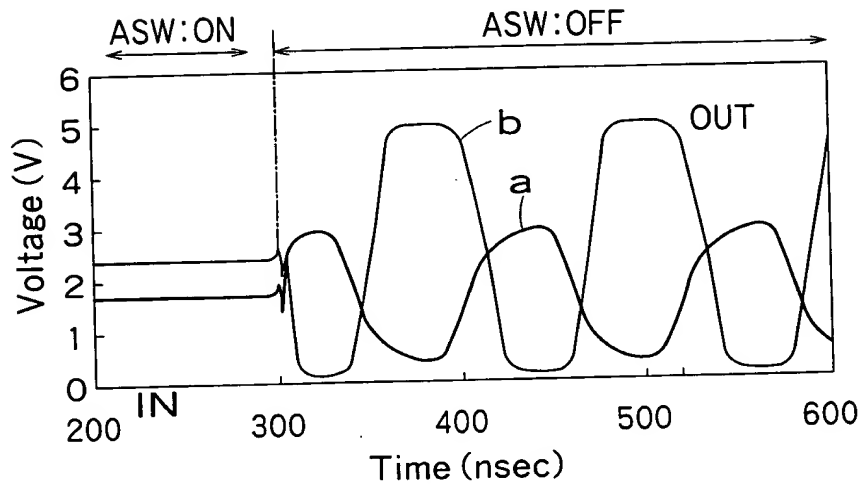


FIG. 11

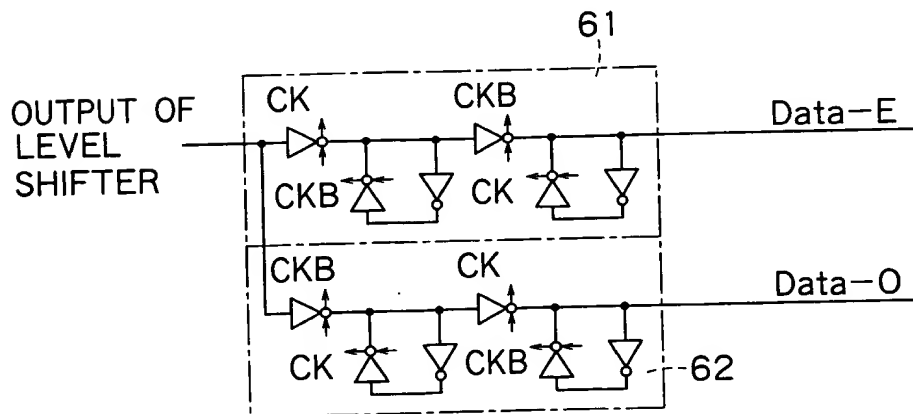


FIG. 12

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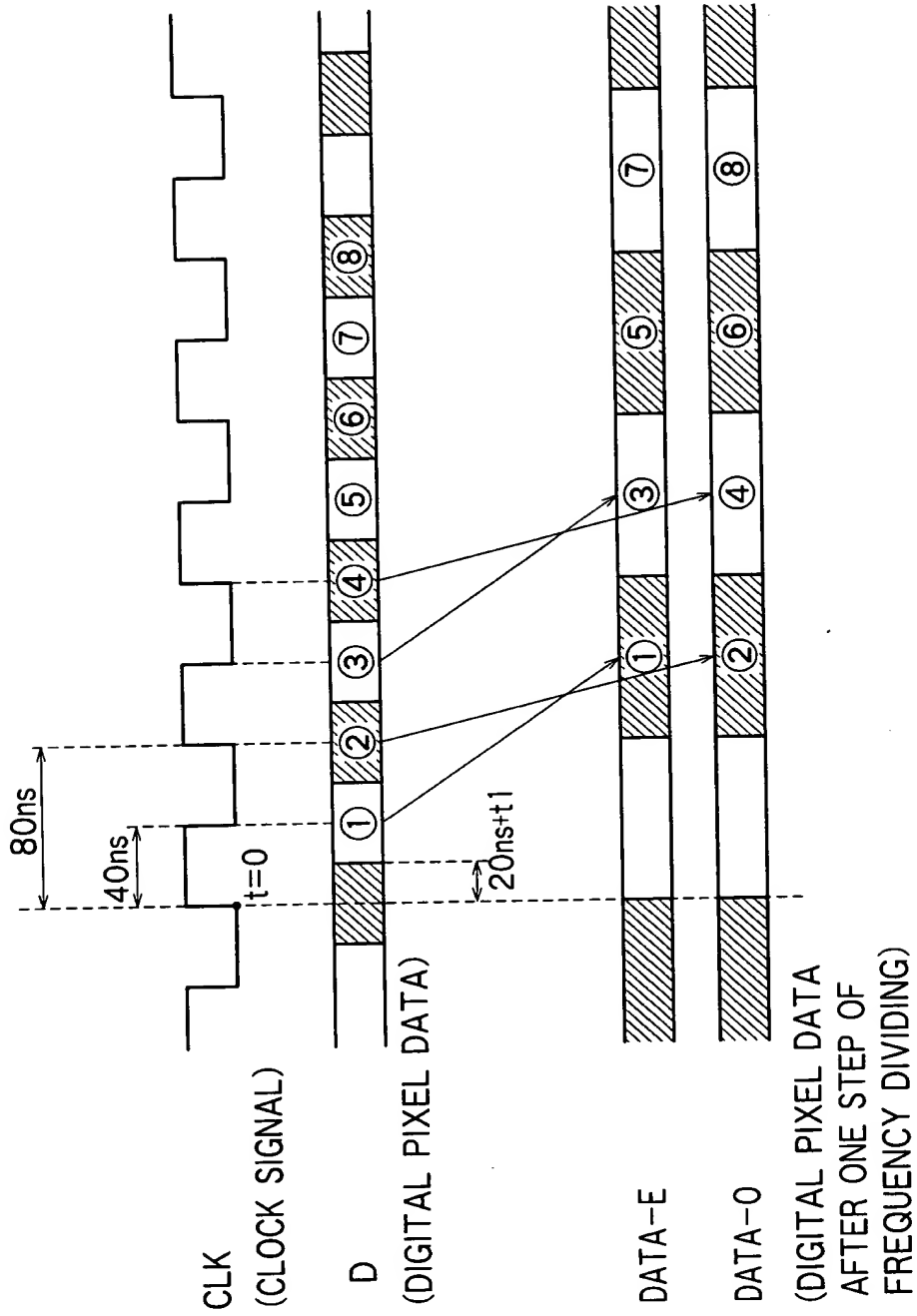


FIG. 13

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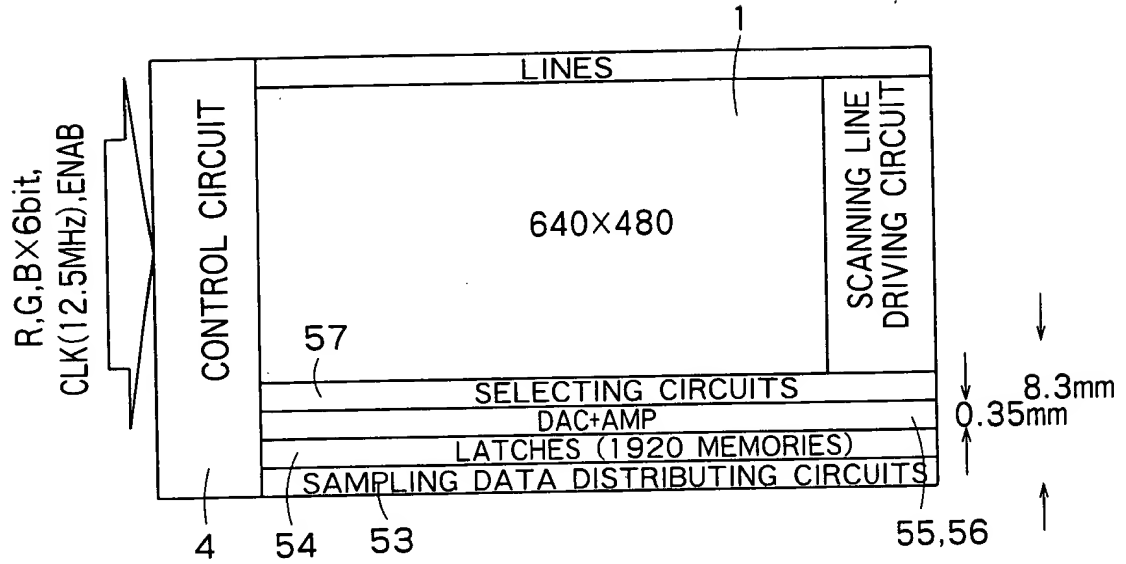


FIG. 14

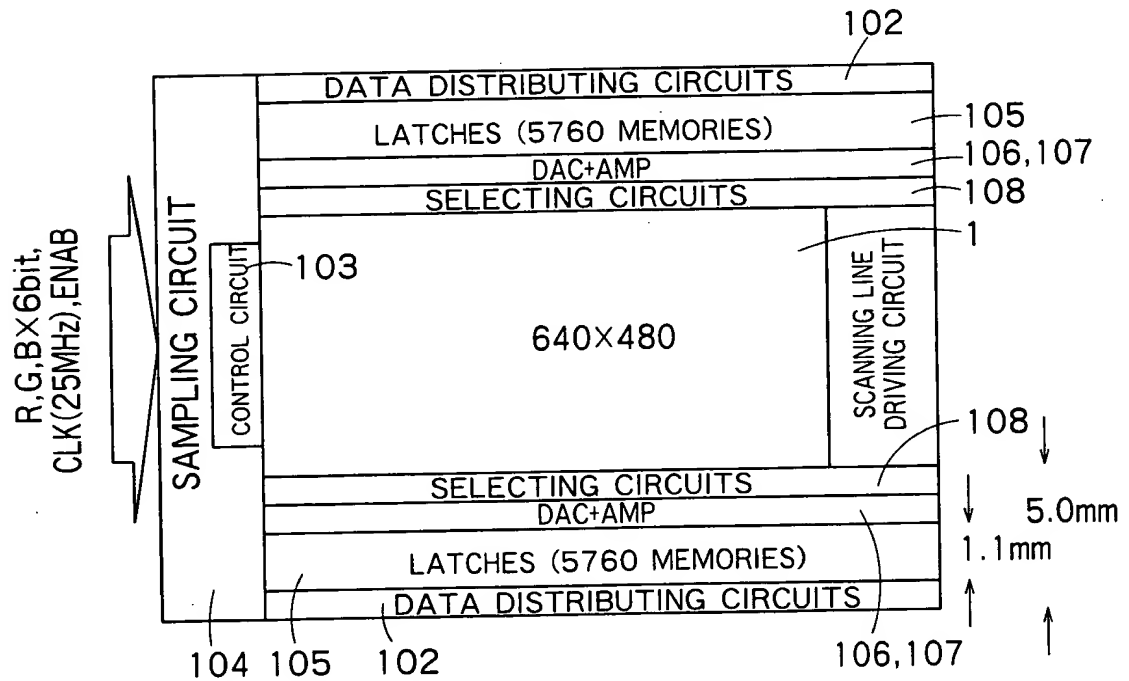


FIG. 15

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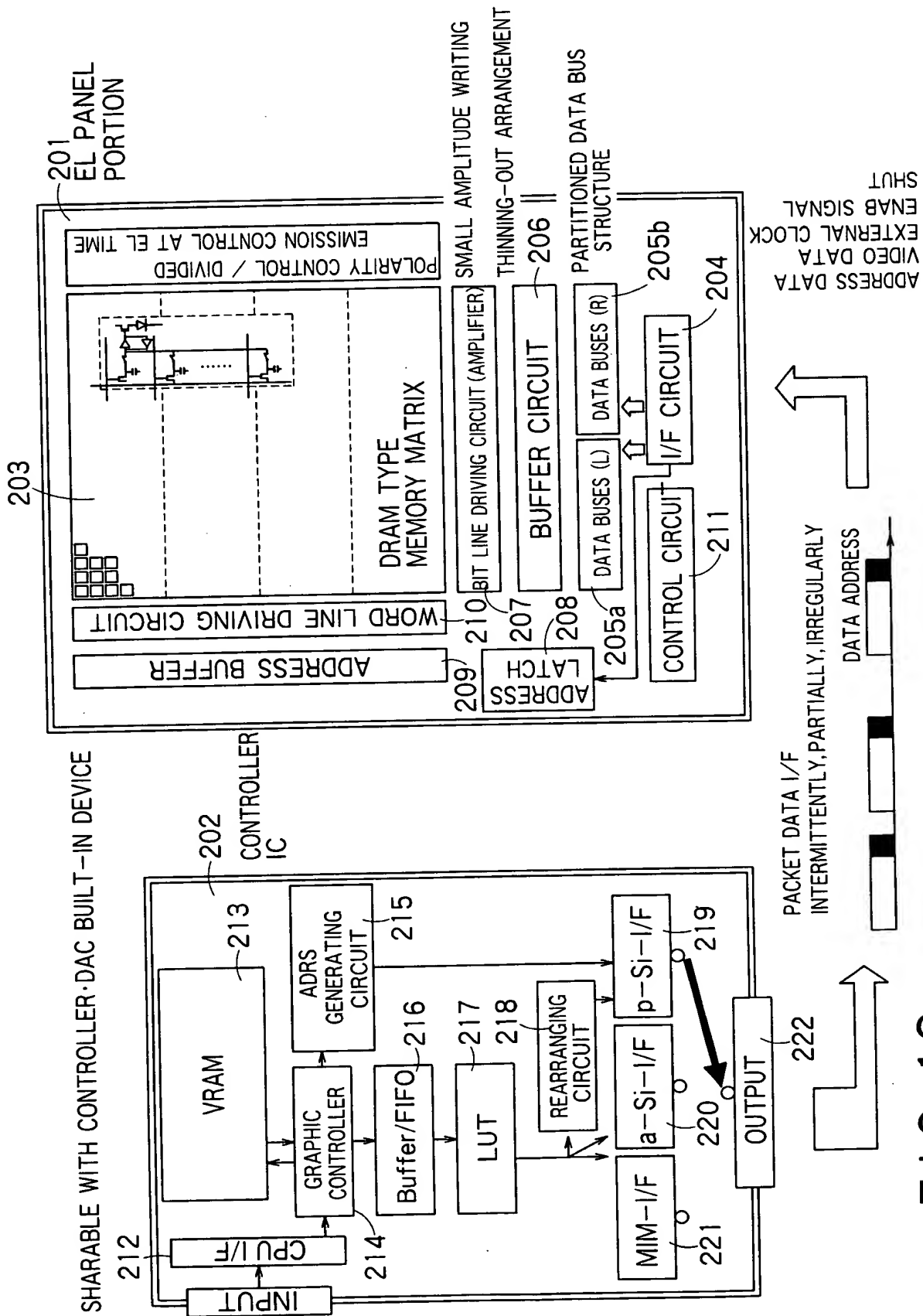
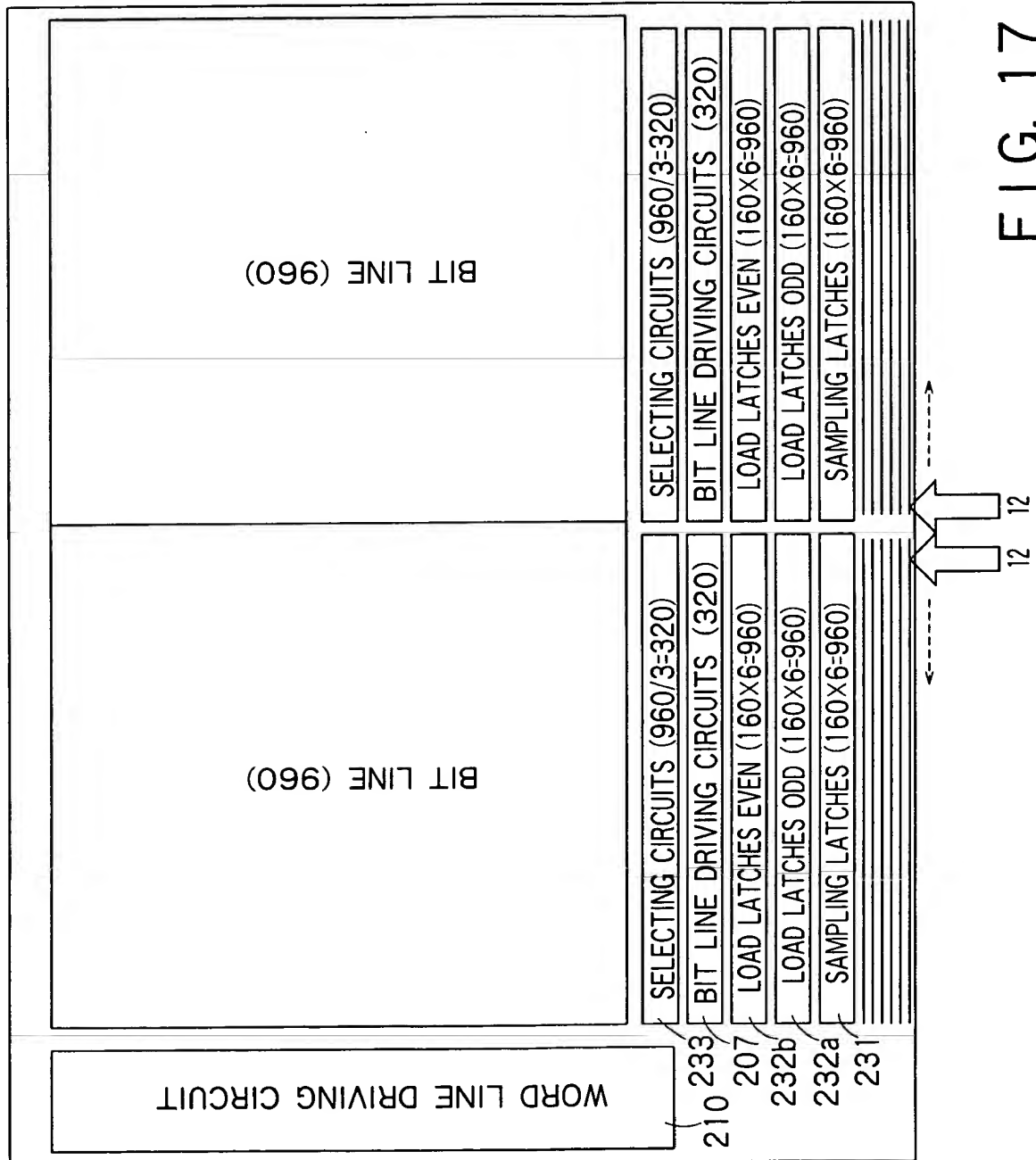


FIG. 16



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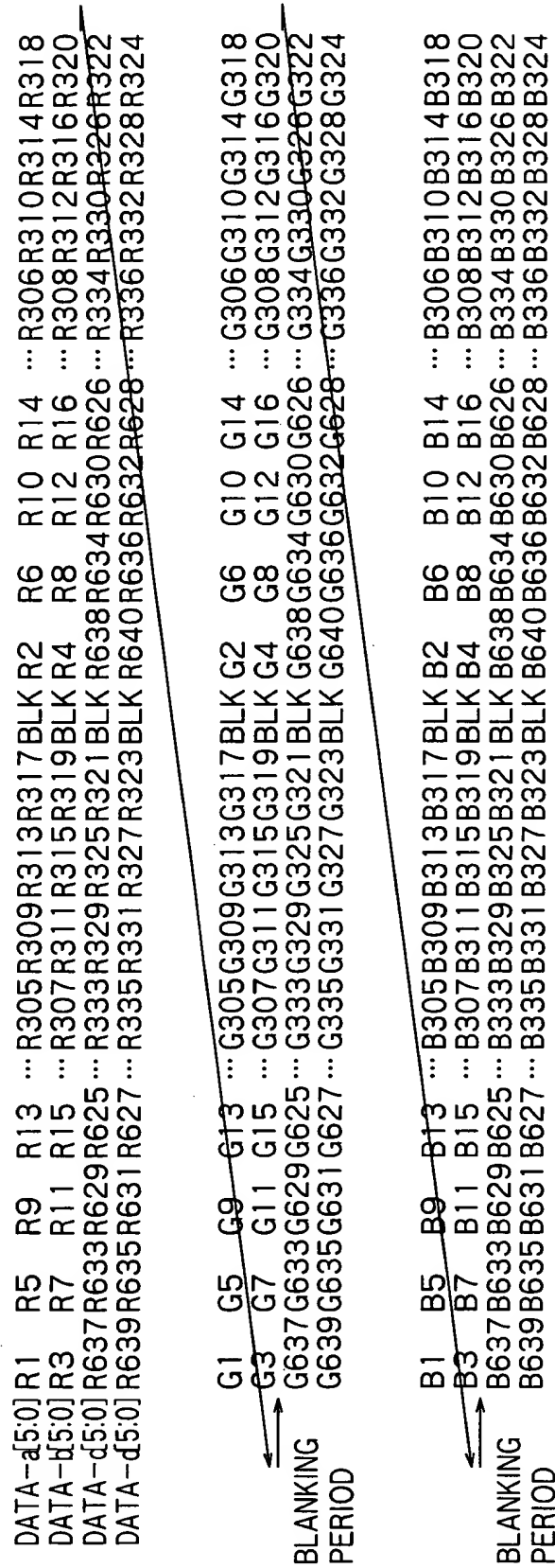


FIG. 18

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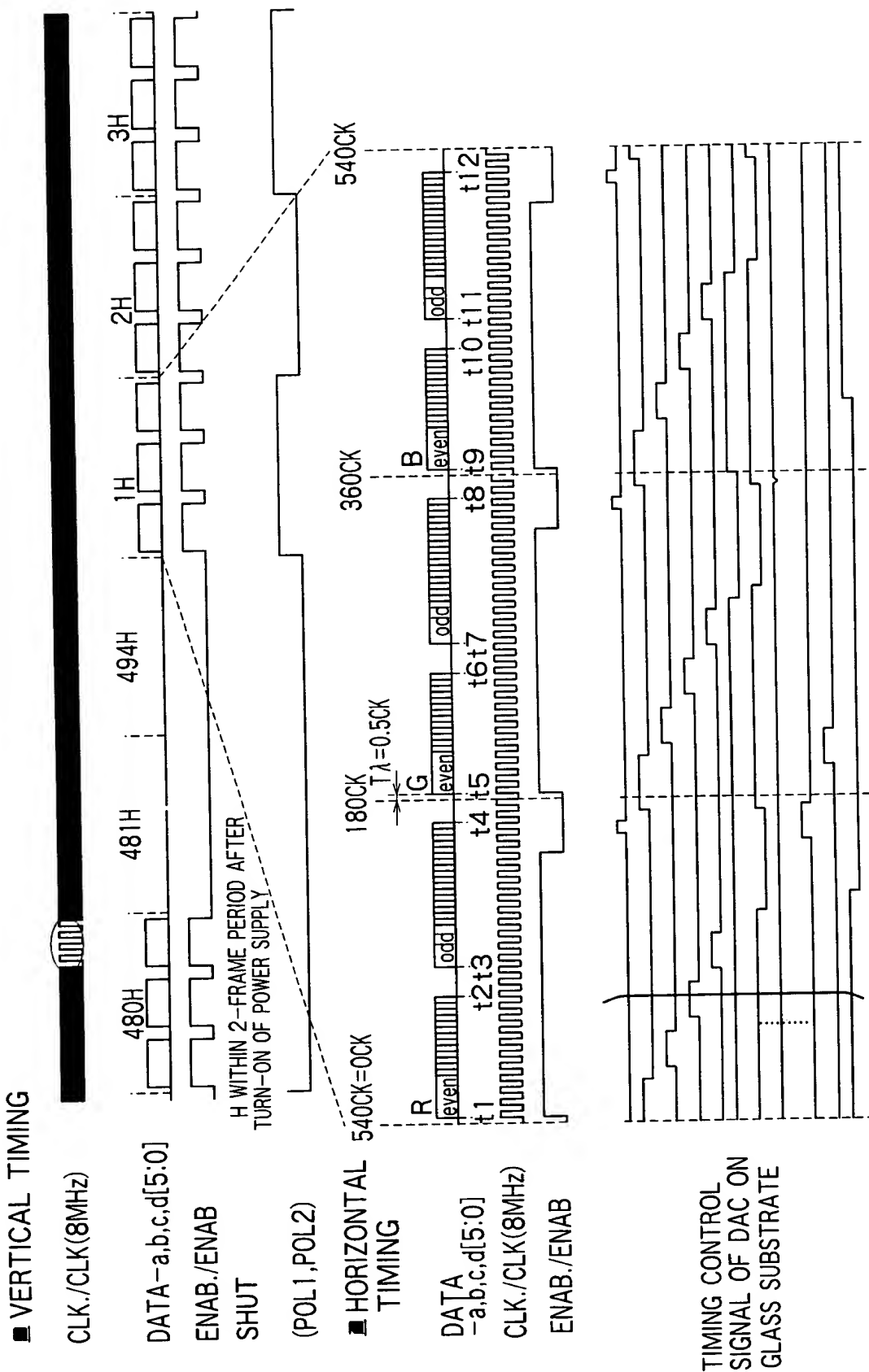


FIG. 19

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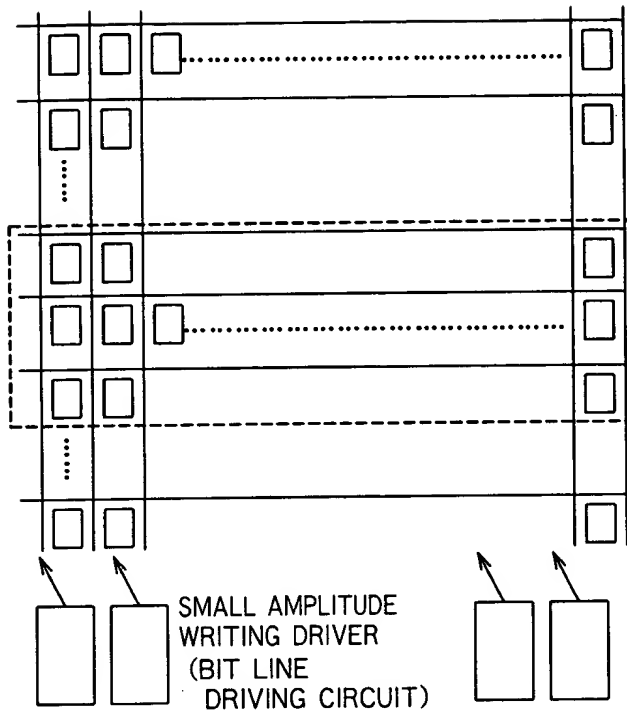


FIG. 20A

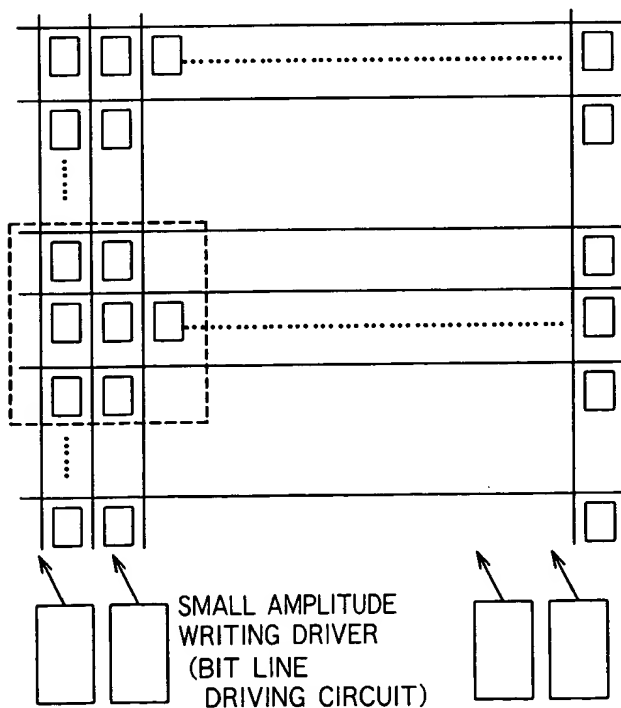


FIG. 20B

206608US2

## ■ VERTICAL TIMING

[illegible]

H WITHIN 2-FRAME PERIOD AFTER  
TURN-ON OF POWER SUPPLY

[illegible][illegible]

FIG. 21



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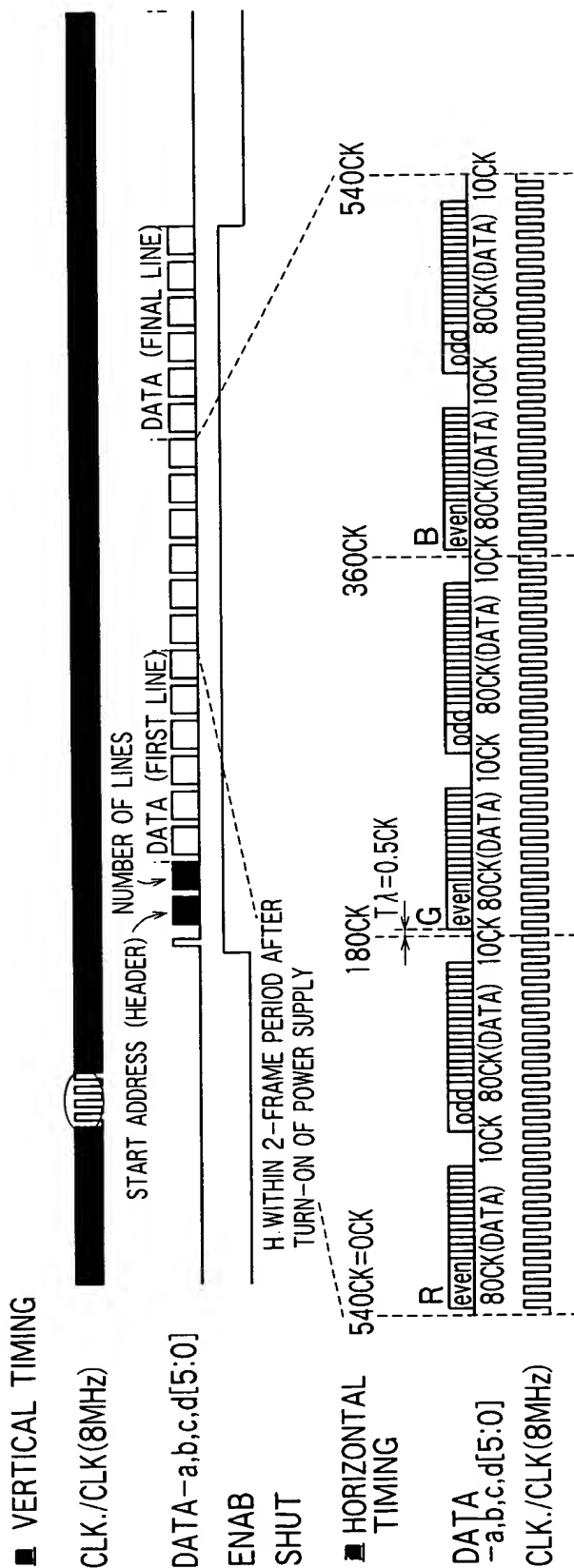


FIG. 22

CASE IN WHICH ONE DAC IS PROVIDED EVERY 6 SIGNAL LINES (1)

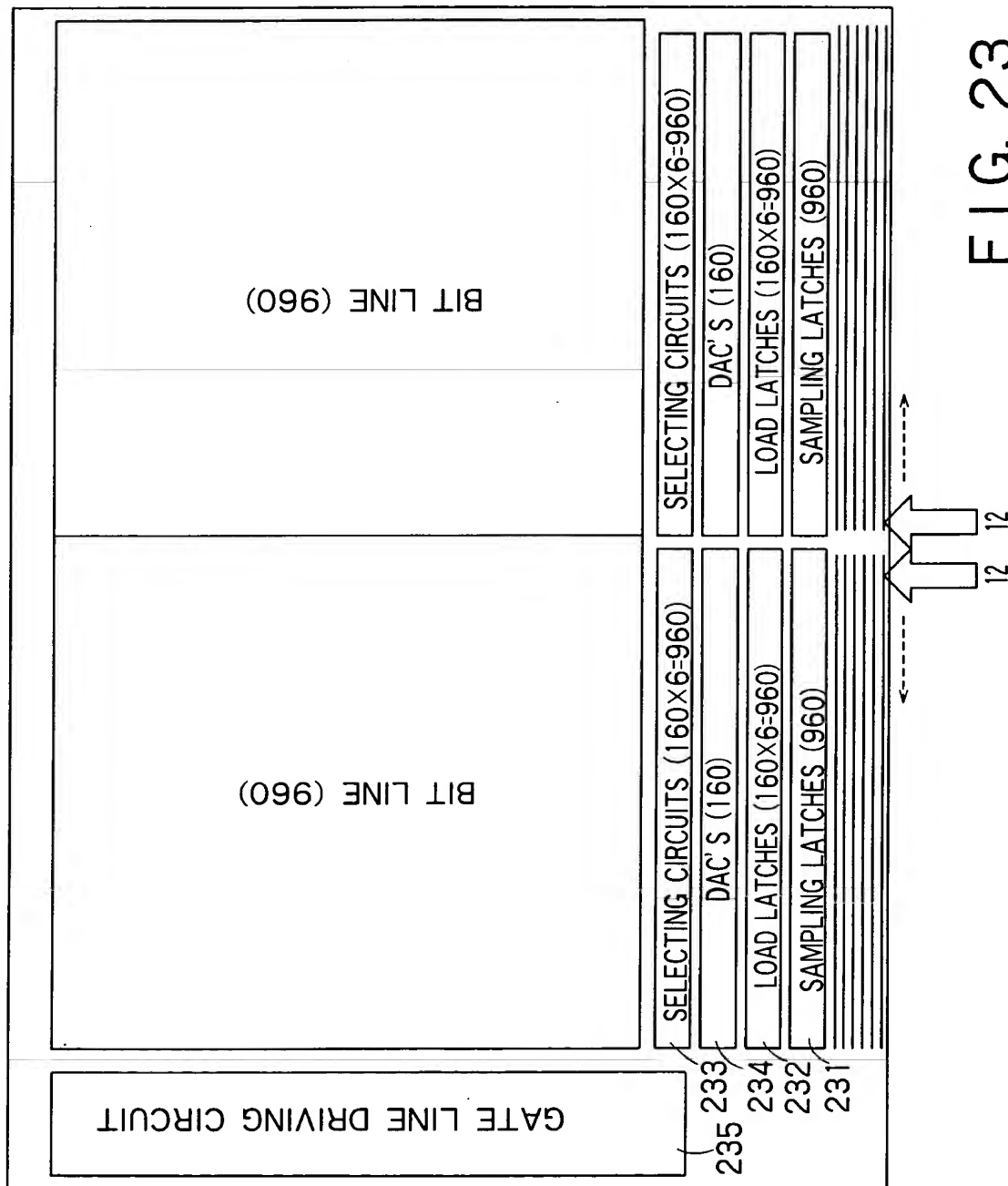


FIG. 23

CASE IN WHICH ONE DAC IS PROVIDED EVERY 3 SIGNAL LINES (1)

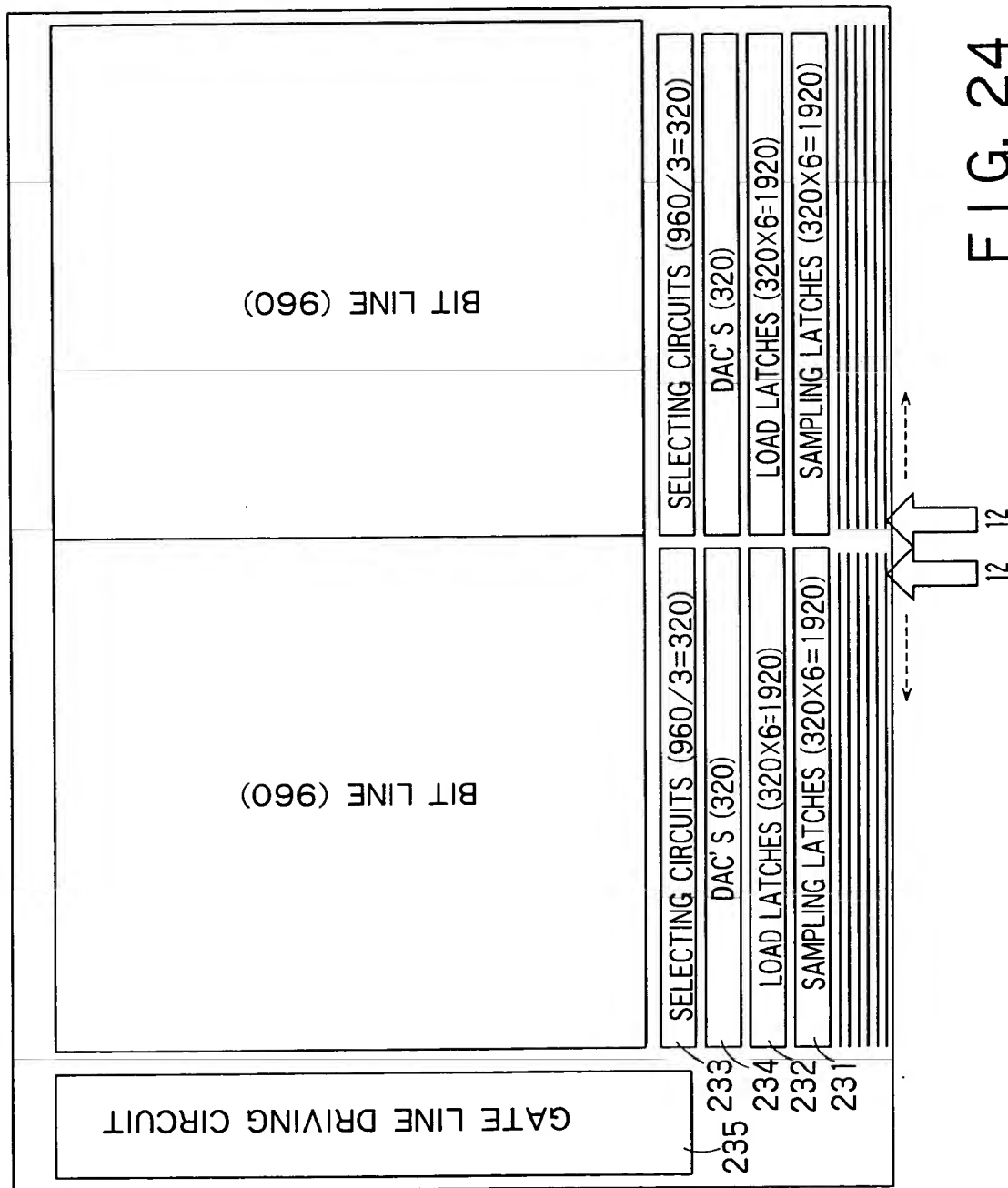


FIG. 24

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FIG. 25

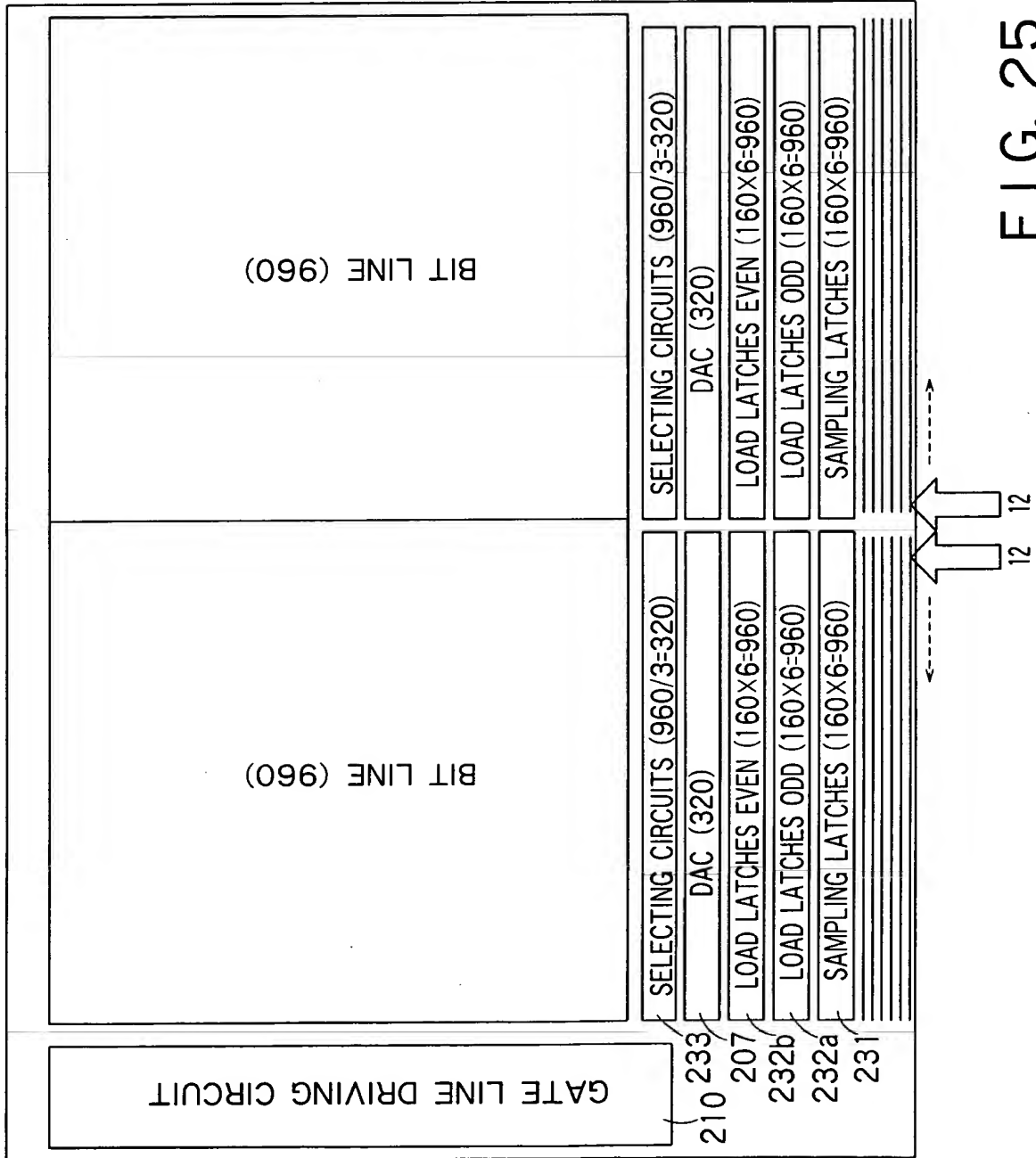


FIG. 25

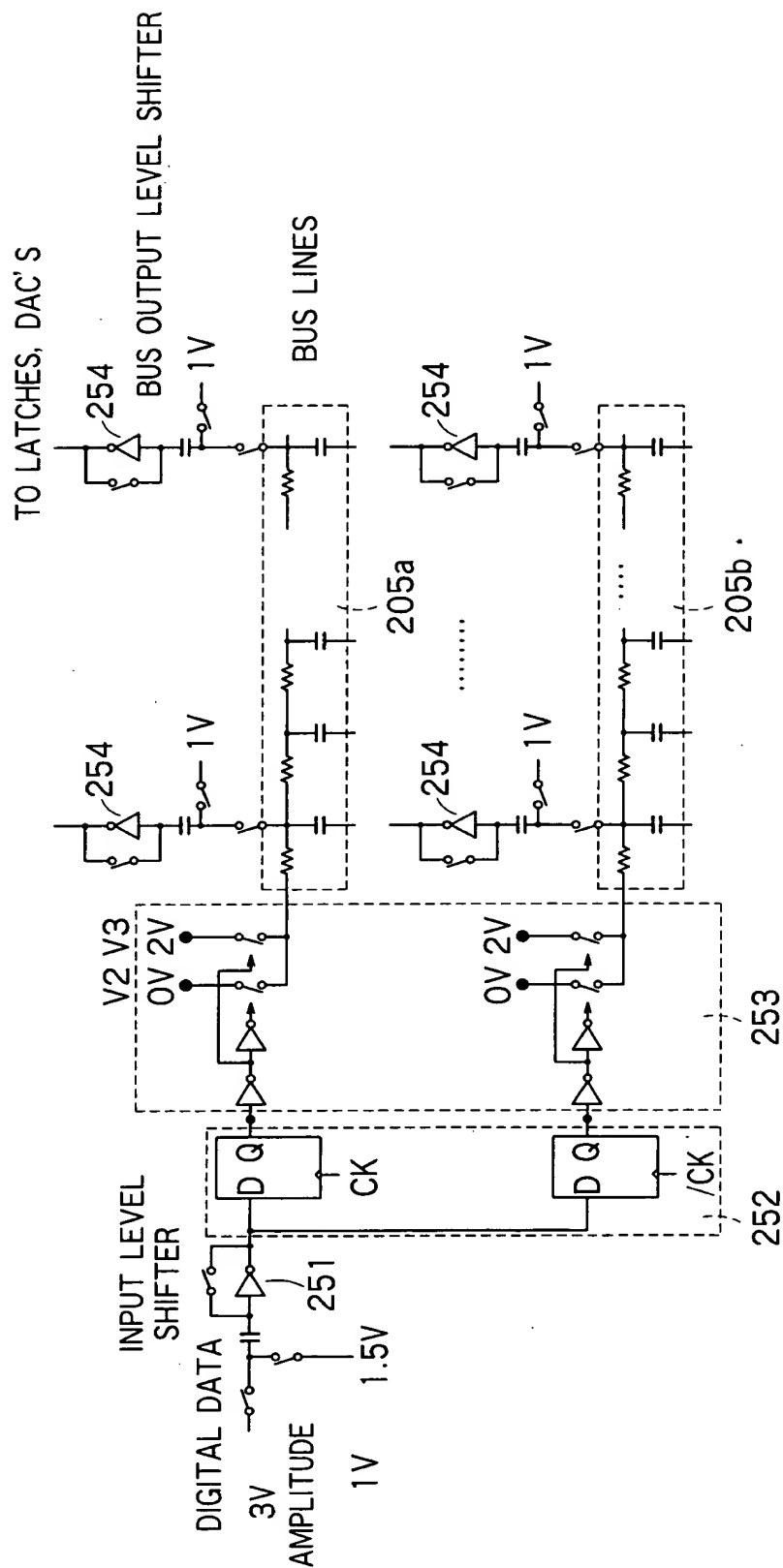


FIG. 26

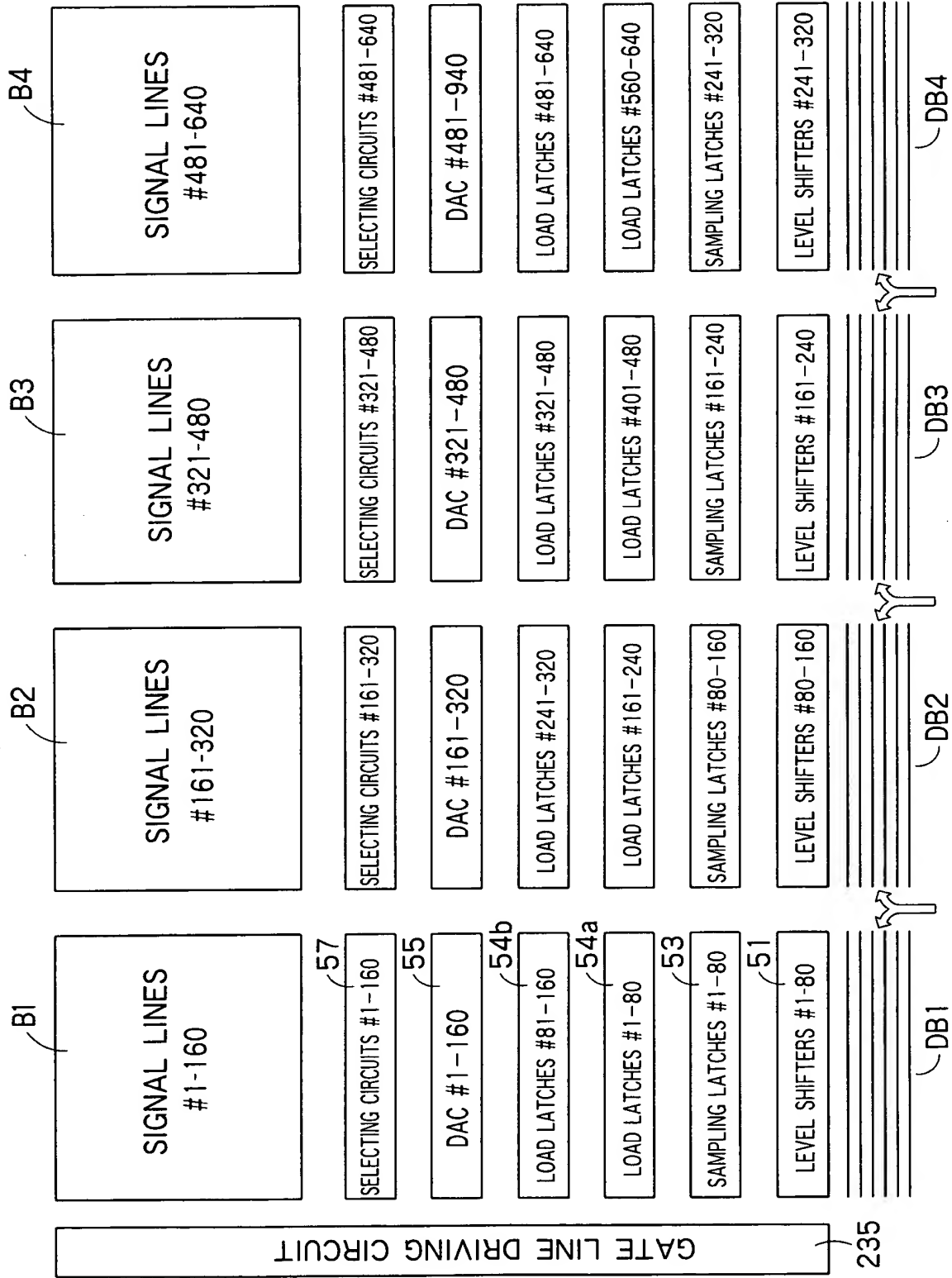


FIG. 27

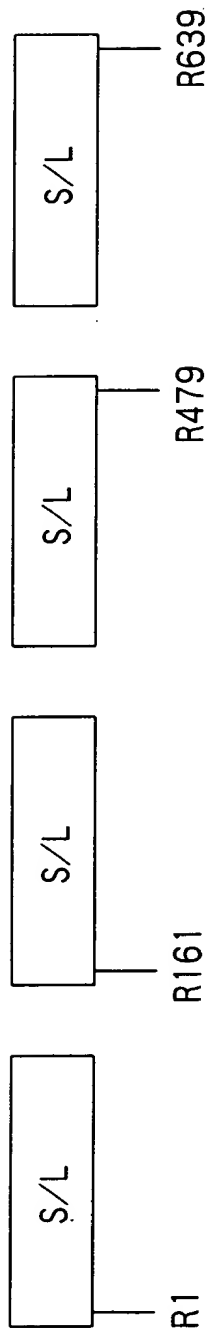


FIG. 28A

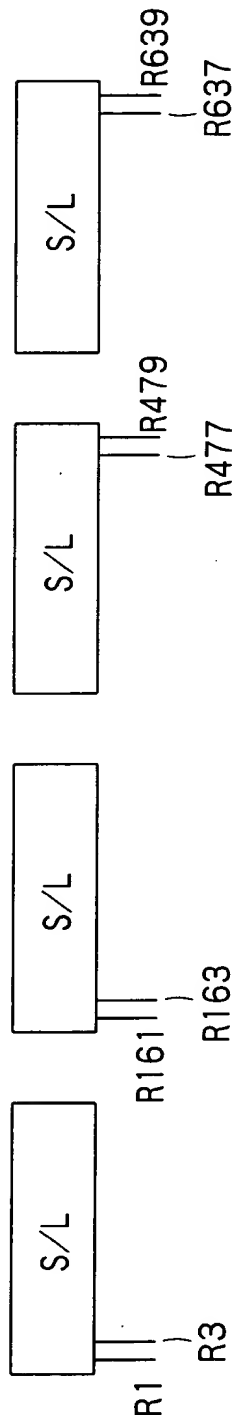


FIG. 28B

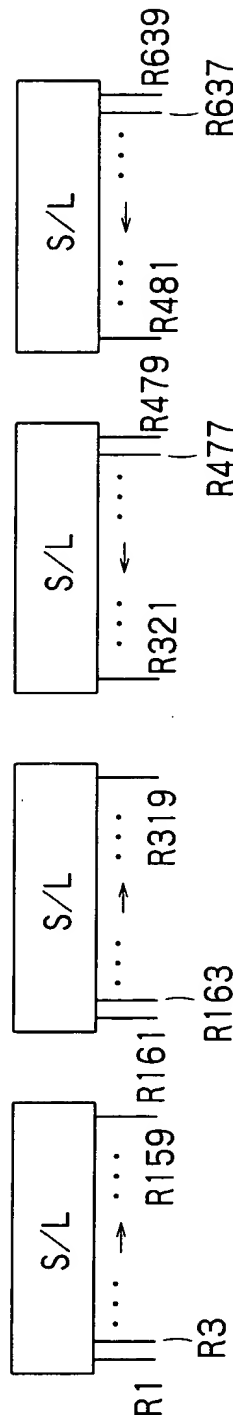


FIG. 28C

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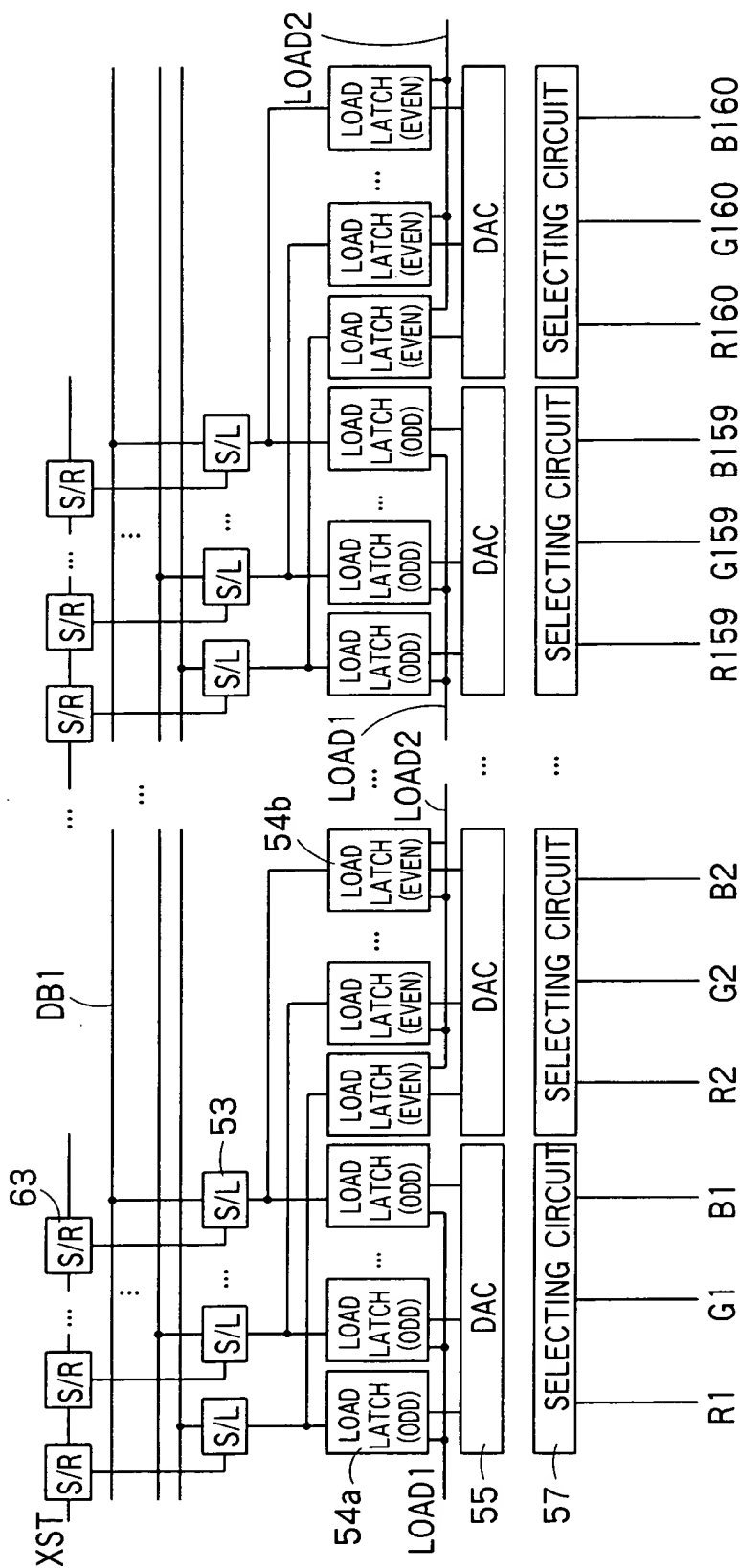


FIG. 29



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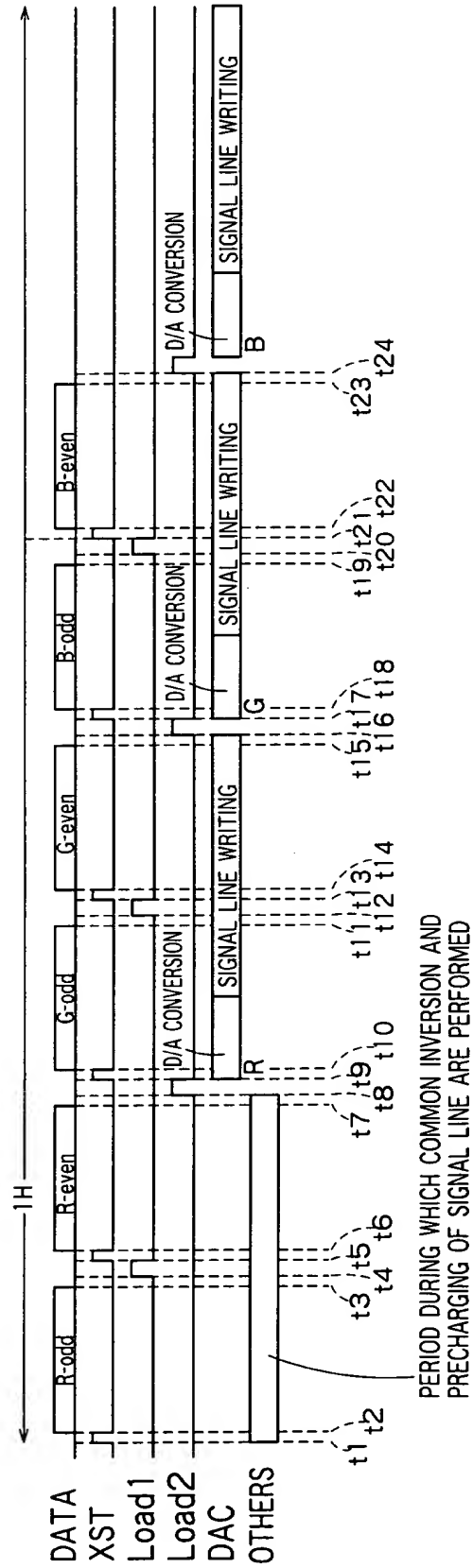


FIG. 30

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FIG. 30

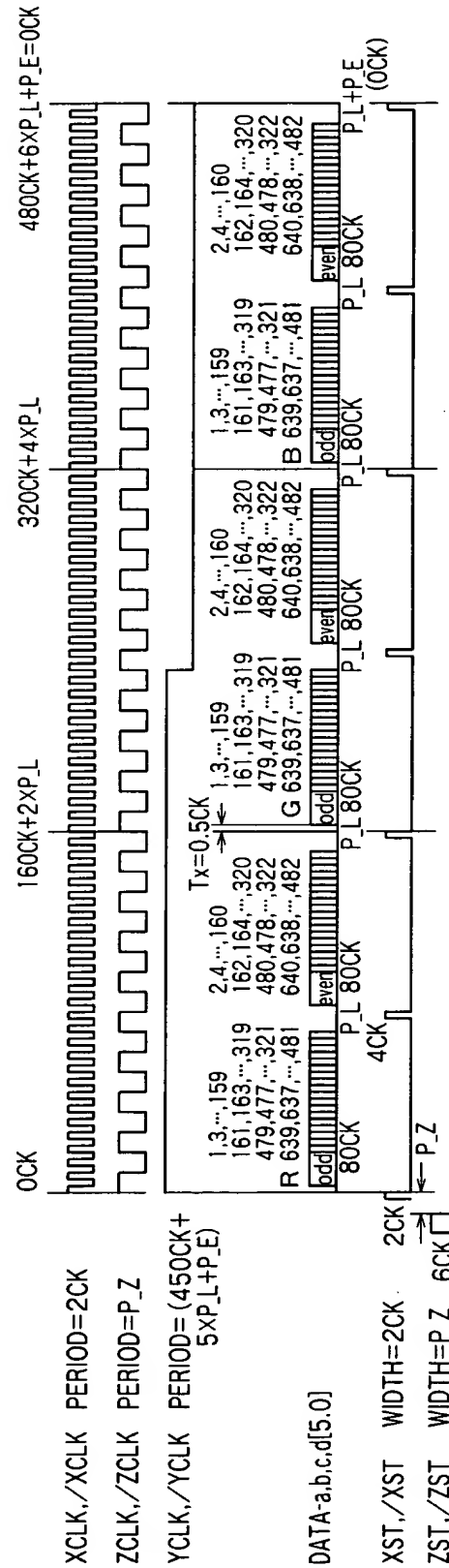


FIG. 31

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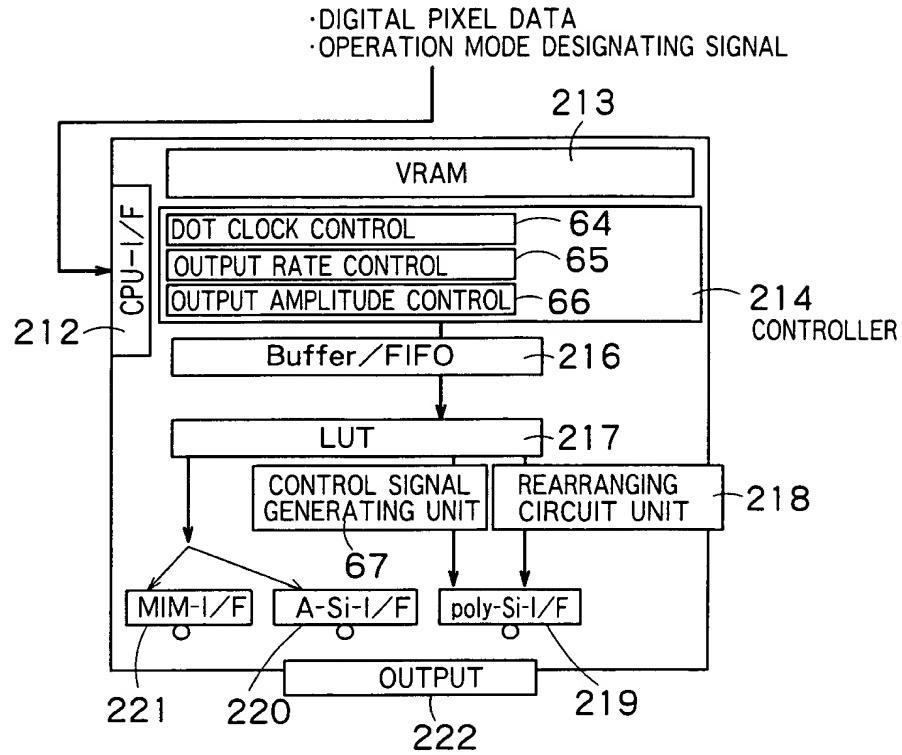


FIG. 32

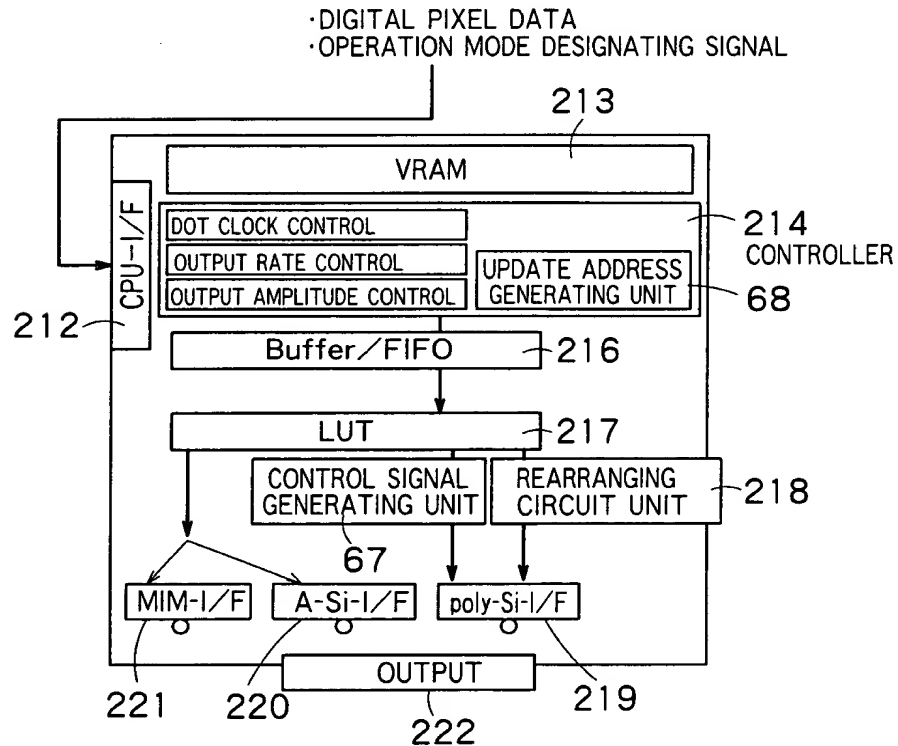


FIG. 33

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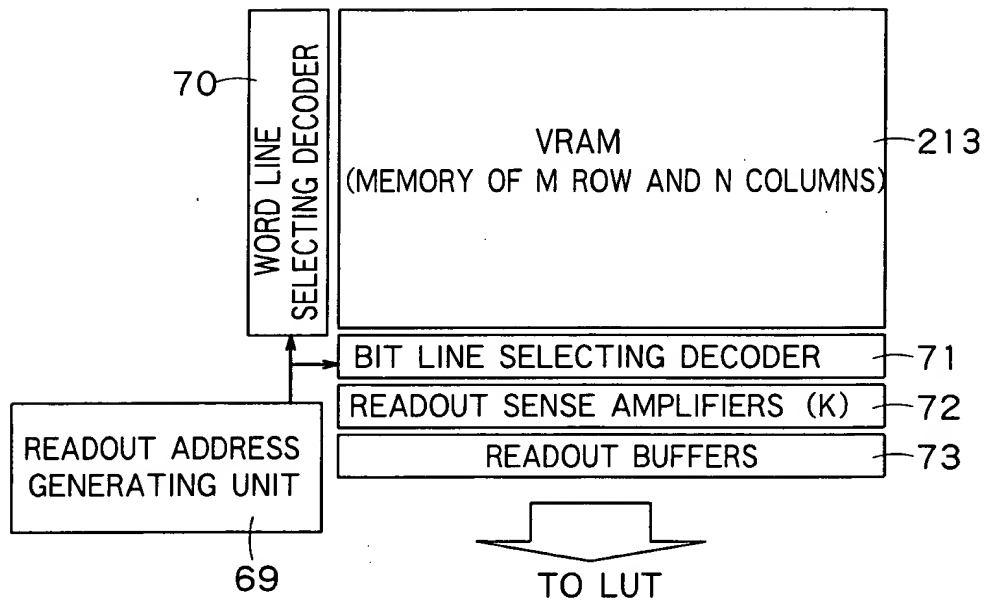


FIG. 34

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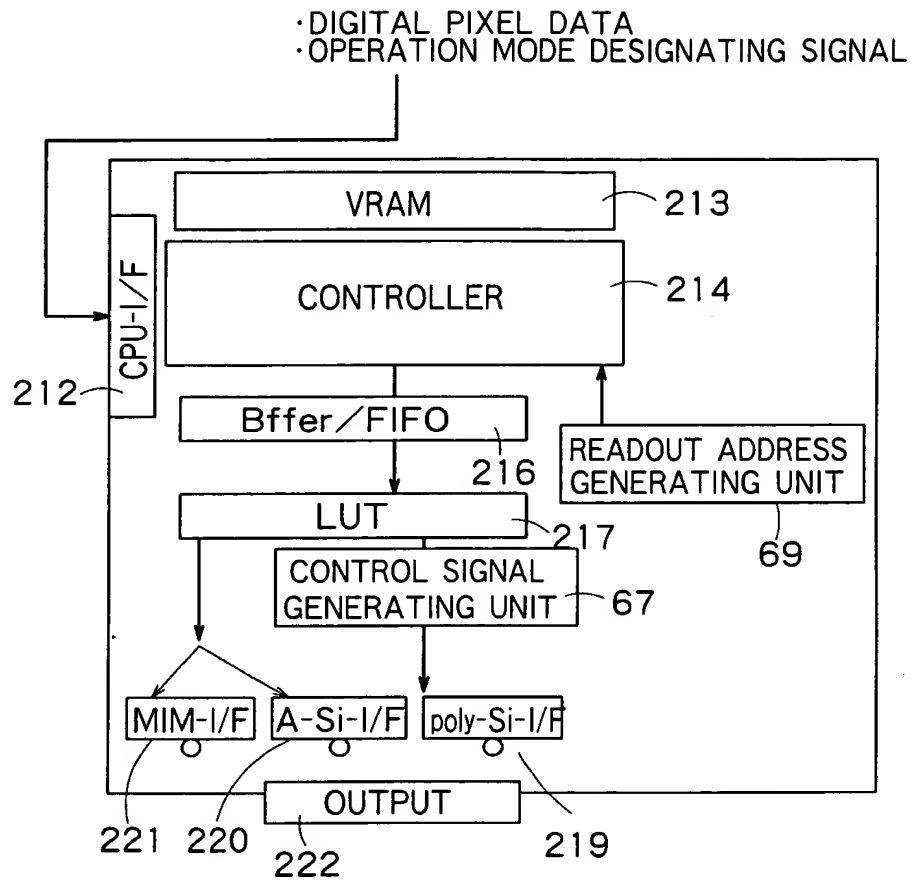


FIG. 35

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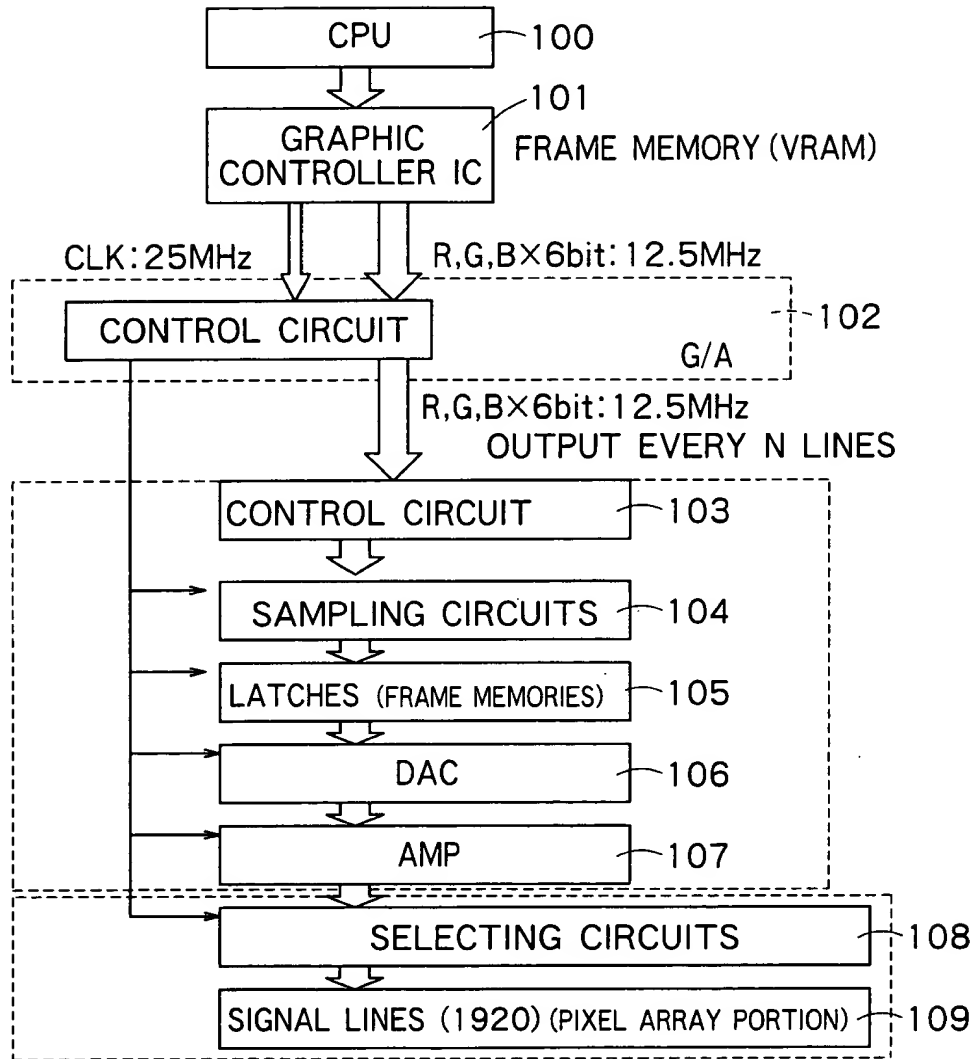


FIG. 36